WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

a first conductive layer formed on an insulating substrate;

a gate insulating layer on the first conductive layer;

a semiconductor layer on the gate insulating layer;

a second conductive layer formed at least in part on the semiconductor layer and including a data line and a drain electrode separated from each other, the second conductive layer including a lower film of barrier metal and an upper film of Al or Al alloy;

a passivation layer covering the semiconductor layer; and

a third conductive layer formed on the second conductive layer and contacting the second conductive layer,

wherein at least an edge of the upper film lies on the lower film such that the lower film includes a first portion exposed out of the upper film, and the third conductive layer contacts the first portion of the lower film.

2. The thin film transistor array panel of claim 1, wherein an edge of the upper film traverses the lower film.

3. The thin film transistor array panel of claim 1, wherein the passivation layer has a contact hole exposing the first portion of the lower layer at least in part,

at least a portion of the third conductive layer is located on the passivation layer, and

the at least an edge of the upper film does not coincide boundary of the contact hole.

4. The thin film transistor array panel of claim 3, wherein the passivation layer contacts the lower film near the contact hole.

5. The thin film transistor array panel of claim 1, wherein the lower film comprises Cr, Mo or Mo alloy.

6. The thin film transistor array panel of claim 1, further comprising an ohmic contact interposed between the semiconductor layer and the second conductive layer.

7. The thin film transistor array panel of claim 6, wherein the ohmic contact has substantially the same planar shape as the second conductive layer.

8. The thin film transistor array panel of claim 1, wherein boundary of the semiconductor layer either substantially coincides with boundary of the second conductive layer or is located outside the second conductive layer.

9. The thin film transistor array panel of claim 1, wherein the third conductive layer comprises ITO or IZO.

10. The thin film transistor array panel of claim 1, wherein the third conductive layer comprises a pixel electrode contacting the drain electrode.

11. The thin film transistor array panel of claim 10, wherein the passivation layer has a first contact hole for contact between the drain electrode and the pixel electrode, a second contact hole exposing a portion of the first conductive layer, and a third contact hole exposing a portion of the data line, and the third conductive layer comprises a first contact assistant contacting the first conductive layer through the second contact hole and a second contact assistant contacting the data line through the third contact hole.

12. The thin film transistor array panel of claim 1, wherein the first portion of the second conductive layer has unevenness.

13. A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate conductive layer on an insulating substrate;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data conductive layer including a data line and a drain electrode separated from each other and a double-layered structure including a lower film and an upper film;

removing a first portion of the upper film to expose a first portion of the lower film; and

forming a pixel conductive layer contacting the first portion of the lower film,

wherein the formation of the semiconductor layer is performed by using a photoresist and the removal of the first portion of the upper film is performed by using the photoresist as an etch mask.

14. The method of claim 13, wherein the lower film comprises a barrier metal, and the upper film comprises Al or Al alloy.

15. The thin film transistor array panel of claim 13, further comprising:

forming an ohmic contact between the semiconductor layer and the data conductive layer.

16. The method of claim 13, wherein the formation of the semiconductor layer and the data conductive layer comprises:

depositing an amorphous silicon layer;

forming the data conductive layer on the amorphous silicon layer, the data conductive layer including the lower film and the upper film;

coating a photoresist on the upper film and the amorphous silicon layer;

removing a first portion of the upper film, the first portion being exposed out of the photoresist; and

forming the semiconductor layer including the amorphous silicon layer by removing portions of the amorphous silicon layer exposed out of the data conductive layer and the photoresist.

17. The method of claim 16, wherein the first portion of the upper film is not covered with the photoresist, the semiconductor layer includes a channel portion located between the data line and the drain electrode, and the photoresist covers the channel portion.

18. The method of claim 17, wherein the amorphous silicon layer includes an intrinsic amorphous silicon film and an extrinsic amorphous silicon film on the intrinsic amorphous silicon film, and further comprising:

removing the photoresist after the formation of the semiconductor layer; and

removing portions of the extrinsic amorphous silicon film exposed out of the data conductive layer.

19. The method of claim 18, further comprising:

leaving an island-like portion of the upper film on the lower film; and

removing the island-like portion of the upper film by blanket etch.

20. A thin film transistor array panel comprising:

a gate conductive layer formed on an insulating substrate;

a gate insulating layer on the gate conductive layer;

a semiconductor layer on the gate insulating layer;

a data conductive layer formed at least in part on the semiconductor layer and including a data line and a drain electrode separated from each other;

a passivation layer covering the semiconductor layer; and

a pixel electrode contacting the drain electrode,

wherein boundary of the semiconductor layer is exposed out of the data line except for places near the drain electrode and an end portion of the data line.

21. The thin film transistor array panel of claim 20, wherein the data conductive layer has a multilayered structure including a lower film and an upper film, and the lower film and the upper film have different shapes.

22. The thin film transistor array panel of claim 21, wherein the lower film comprises a barrier metal and the upper film comprises Al or Al alloy.

23. The thin film transistor array panel of claim 20, wherein the data line has an edge substantially parallel to the semiconductor layer, the edge of the data line either placed on the semiconductor layer or coinciding with an edge of the semiconductor layer.

24. The thin film transistor array panel of claim 23, wherein the pixel electrode has an edge overlapping the gate conductive layer, the data conductive layer, or the semiconductor layer.

25. The thin film transistor array panel of claim 20, further comprising an ohmic contact interposed between the semiconductor layer and the data conductive layer and having substantially the same planar shape as the data conductive layer.

26. The thin film transistor array panel of claim 20, wherein a lateral side of the data conductive layer is tapered.

27. The thin film transistor array panel of claim 20, wherein the passivation layer has a first contact hole for contact between the drain electrode and the pixel electrode, a second contact hole exposing a portion of the gate conductive layer, and a third contact hole exposing a portion of the data line, and further comprising:

a first contact assistant contacting the gate conductive layer through the second contact hole and a second contact assistant contacting the data line through the

third contact hole, the first and the second contact including the same layer as the pixel electrode.

28. The thin film transistor array panel of claim 27, wherein the passivation layer contacts the lower film near the first and the second contact holes.

29. The thin film transistor array panel of claim 20, wherein a portion of the drain electrode contacting the pixel electrode has unevenness.

30. A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate line on an insulating substrate;

forming a gate insulating layer on the gate line;

forming a semiconductor layer on the gate insulating layer;

forming a data conductive layer including a data line intersecting the gate line and a drain electrode separated from the data line;

forming a pixel conductive layer contacting the drain electrode,

wherein the formation of the semiconductor layer is performed by using a photoresist as an etch mask and the photoresist does not cover a portion of the data conductive layer.

31. The method of claim 30, wherein the data line and the drain electrode include a lower film and an upper film.

32. The method of claim 31, further comprising:

removing the uncovered portion of the upper film.

33. The method of claim 13, wherein the formation of the semiconductor layer and the data conductive layer comprises:

depositing an amorphous silicon layer;

forming the data conductive layer on the amorphous silicon layer, the data conductive layer including the lower film and the upper film;

forming the photoresist on the upper film and the amorphous silicon layer;

removing the uncovered portion of the upper film; and

forming the semiconductor layer including the amorphous silicon layer by removing portions of the amorphous silicon layer exposed out of the data conductive layer and the photoresist.

34. The method of claim 33, further comprising:

leaving an island-like portion of the upper film on the lower film; and

removing the island-like portion of the upper film by blanket etch.

35. The method of claim 30, wherein the semiconductor layer includes a channel portion located between the data line and the drain electrode and the photoresist covers the channel portion.